09/735,944
Art Unit: 2634

**Remarks**

The applicants have amended the claims to overcome the formal objections. Claim 24 has been cancelled, thus obviating the need for the drawing amendment. Claims 17 and 19 have been amended as suggested by the Examiner. Claim 19 has been corrected to indicate that it is the outputs of the comparators that are input to the counter. Claim 20 has been amended so as to only refer to the error flag as shown in Figure 8.

The reference to weighted output has been removed from claim 7, and claim 16 has been cancelled.

The word adder in claim 21 has been replaced by accumulator as used in claim 19.

With regard to the rejection under 35 USC 102, claim 1 has been amended to more clearly define the invention as being directed to a multimode clock recovery circuit that can provide a recovered clock signal from diverse input signals, including a line rate signal in line rate mode, an SRTS signal in SRTS mode, and buffer fill level in an adaptive mode. As described in the specification, in the adaptive mode the buffer fill level is used to develop the phase signal that is input to the loop filter to control the DCO. In the SRTS mode, the local SRTS generator forms part of the feedback loop of the PLL. In line rate mode the output of the PLL is fed back directly to the one of the other inputs.

It is believed that claim 1 as amended is not anticipated by Muntz. Contrary to the Examiner's assertion it appears that Muntz does not employ a PLL as claimed. At column 7, line 66, Muntz indicates that the frequency translator 426 can be a PLL, but the applicants can find no reference to Muntz indicating that a PLL is used to recover the clock signals.

In Muntz, the clock generator consists of a low pass filter and an NCO (DCO), but there is no feedback signal shown. The phase error applied to the low pass filter is obtained directly from the STRS unit, (Fig. 4), the buffer fill level (Figure 5), and the network (Figure 6). Figure 7 is merely a composite of Figs. 4, 5, and 6 with a selector 708 to select the desired clock recovery unit. Such an arrangement would not recover clock signals with the accuracy and stability offered by the present invention.

In accordance with the principles of the present invention, the clock recovery circuit includes a PLL with a phase detector having multiple inputs for comparing an input signal with an output signal (no such phase detector is included in Fig. 7 of Muntz). In the SRTS mode, the phase detector (Figure 8) derives the phase signal from locally generated time stamps (based on the output of the PLL) and time stamps received over the network. In adaptive mode, the adaptive clock recovery signal is applied to the low pass filter to control the phase of the DCO. In the adaptive mode, Muntz is similar to the invention in its broad aspect in that that the output of the phase error derived from the buffer fill level is applied to the input of the low pass filter. However, unlike Muntz, the invention employs a PLL with a phase detector having multiple inputs for use in other modes. The use of a PLL offers much more accurate clock recovery and also offers the possibility of placing the recovery circuit in a free running holdover mode when no usable input signal is available.

The prior art does not disclose a multiple input PLL adapted for different kinds of input as taught in the present invention. The ability to use common circuit elements is also a feature of the invention.

It is noted that the Examiner rejected former claim 18 over Munzt in view of Brauns on the basis that Muntz teaches an SRTS generator in a feedback loop, claiming that 460 -464- 436 constitute the loop. However, a feedback loop by definition requires an output signal to be fed back to an input signal. 460 -464- 436 does not constitute such a loop because in these elements there is no path wherein an output signal can be returned to the input. Figure 4 of Muntz discloses a non PLL implementation wherein a time stamp is generated from a received SRTS signal, and this is used to control the NCO 460 via the low pass filter 456. There is no teaching of generating a local SRTS signal from the output of a PLL and deriving a phase signal from the locally generated SRTS signal and the received SRTS signal as illustrated in Figure 8. Claim 18 has been clarified to make it clear that the phase detector derives the phase signal from the locally generated SRTS signal and the incoming SRTS signal. Muntz does not disclose this. A combination of Brauns and Muntz does not result in claim 18 as presently defined.

The Examiner rejected former claim 19 over Bleiweiss, which in Figure 4 appears to show a local SRTS generator in a feedback loop. However, Bleiweiss does not address the problem of the false behaviour arising as a result of the fact that the counters used to generate the SRTS

values include a modulo function, which would give rise to a sawtooth effect. In accordance with the principles of one aspect of the invention, this problem is overcome by including the weighted up/down counter, which in effect keeps track of the number of wrap-arounds (see lines 6 – 13 of the specification). This is not taught in the prior art.

The examiner rejected former claim 10 in part over Bleiweiss on the basis that the counter is provided by 151 to 155-157-161. However, the applicants can find no reference in Figure 6 of Bleiweiss to a non wrap-around up/down counter, which as noted above is required to overcome the sawtooth effect that would otherwise occur by keeping track of the number of wrap-arounds.

It is believed that this application is in condition for allowance. Allowance and reconsideration are earnestly solicited.

Respectfully submitted,

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